# CS Masters' Thesis Defense

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| **Title:** | *Making a Flash Translation Layer Reliability-Aware: An Optimized Strategy for Wear-Leveling and Garbage-Collection* |
| **Speaker:** | Jonathan Tjioe |
| **Date:** | Tuesday, August 30, 2011 |
| **Time:** | 2:00 p.m. |
| **Location:** | GMCS 405 |
| **Thesis advisor:** | Dr Tao Xie |

**Abstract:**
NAND flash memory has been widely used in the consumer market because of its desirable properties such as low access latency and high energy-efficiency. The NAND flash memory based solid state disk (SSD), which employs a software component called FTL (flash translation layer) to mimic the interface of a hard disk drive (HDD), is considered as a replacement for rotating-based HDD in large-scale enterprise storage systems. Since NAND flash memory has some inherent limitations like out-of-place updates and coarse granularity of erase unit, a variety of FTL techniques have been proposed to greatly overcome the shortcomings. However, most existing FTL schemes only focus on improving performance. We believe that flash SSDs should be fast yet highly reliable.
In this thesis, we propose an optimized strategy named RA (reliability-aware) for flash SSDs to escalate reliability by optimizing wear-leveling and enhancing performance by improving the efficiency of garbage collection. The main principles of RA are: 1) Group cold and hot data in order to improve performance and 2) Select victim blocks so that reliability increases while maintaining fast performance. To demonstrate the effectiveness of RA, we integrate it into two mainstream FTLs: Demand-based Flash Transition Layer (DFTL) and Page Mapping (PM) FTL. We also largely extend a well-known SSD Simulator, FlashSim, in order to implement RA-DFTL and RA-PM. Comprehensive experimental results show that RA-DFTL and RA-PM far exceed the reliability of DFTL and PM while maintaining a similar performance.